Please replace the paragraph beginning on page 1, line 18 with the following new paragraph:

In recent years, DRAM devices employing memory cells each consisting essentially of a single transistor and a single capacitor, also known as "1-transistor/1-capacitor" cells, are becoming denser in integration or "bit-packing" density virtually endlessly. On-chip areas of such memory cells are made smaller once per development of a new generation of products. One basic approach to reducing cell areas is to lower the occupation areas of transistors and capacitors, which make up the cells, respectively.

Please replace the paragraph beginning on page 3, line 16 with the following new paragraph:

High-density DRAM cell structures capable of avoiding these problems have been proposed until today, one of which is disclosed in U. Gruening et al., "A Novel Trench DRAM Cell with a VERtIcal Access Transistor and BuriEd STrap (VERI BEST) for 4Gb/16Gb," IEDM Tech. Dig., 1999. This trench DRAM cell is arranged so that a capacitor is formed at a lower part of a trench defined in a substrate while forming, at an upper part of the trench, a vertically structured transistor with a trench side face as its channel.

Please replace the paragraph beginning on page 5, line 23 and ending on page 6, line 17 with the following new paragraph:

A semiconductor device in accordance with one aspect of the present invention has: an element substrate including a semiconductor layer of a first conductivity type being insulatively formed over a semiconductor substrate with a dielectric film interposed therebetween; said element substrate having a groove formed therein with a depth extending from a top surface of said semiconductor layer into said dielectric film, said groove being formed to have an increased width portion in said dielectric film as to expose a bottom surface of said semiconductor layer; an impurity diffusion source buried in said increased width portion of said groove to be contacted with said bottom surface of said semiconductor layer; and a transistor having a first diffusion layer of a second conductivity type being formed through impurity diffusion from said impurity diffusion source to said bottom surface of said semiconductor layer, a second diffusion layer of the second conductivity type formed through impurity diffusion to said top surface of said semiconductor layer, and a gate electrode formed at a side face of said groove over said impurity diffusion source with a gate insulation film between said side face and said gate electrode.

Please replace the paragraph beginning on page 6, line 18 and ending on page 7, line 9 with the following new paragraph:

A4

A method of fabricating a semiconductor device in accordance with another aspect of the present invention including: forming a groove in an element substrate having a semiconductor layer of a first conductivity type as insulatively formed over a semiconductor substrate with a dielectric film interposed therebetween, the groove being penetrating the semiconductor layer; selectively etching the dielectric film exposed at the groove to form an increased width portion for permitting exposure of a bottom surface of the semiconductor layer; forming an impurity diffusion source buried in the increased width portion of the groove while letting the impurity diffusion source be in contact with only the bottom surface of the semiconductor layer; forming and burying in the groove a gate electrode along with an underlying gate insulation film; and forming in said semiconductor layer source and drain diffusion layers through impurity diffusion to a top surface and also impurity diffusion to the bottom surface by use of said impurity diffusion source.

Please replace the paragraph beginning on page 9, line 8 with the following new paragraph:

A5

Several embodiments of this invention will now be set forth with reference to the accompanying figures.

Please replace the paragraph beginning on page 9, line 12 with the following new paragraph:

A6

Referring now to Fig. 1, there is shown a plan view of a main part of a trench-capacitor-based dynamic random access memory (DRAM) cell array with half-pitch folded bit line structure in accordance with one embodiment of this invention. Also see Figs. 2 and 3, which depict cross-sectional views of the structure of Fig. 1 as taken along lines I-I' and II-II' respectively.

Please see the attach Appendix for the changes made to effect the above paragraphs.